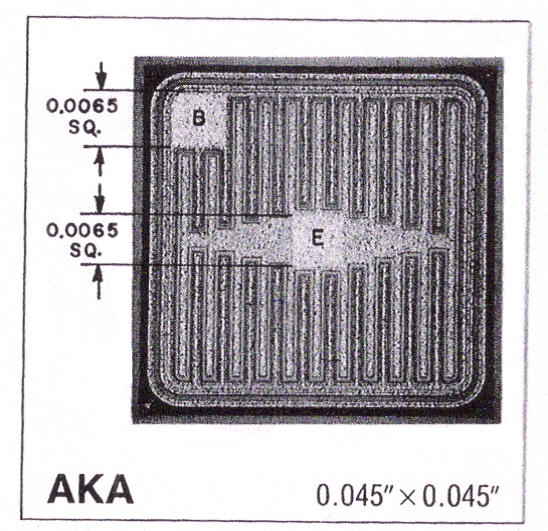
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .0065” X .0065”**

**Backside Potential: Collector**

**Mask Ref: AKA**

**APPROVED BY: DK DIE SIZE .045” X .045” DATE: 10/7/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .011” P/N: 2N3637**

**DG 10.1.2**

#### Rev B, 7/19/02